WHAT IS CLAIMED IS:

1. A silicon controlled rectifier comprising:

a semiconductor region having:

a buried layer having a first conductivity type and a dopant concentration;

a first region having a second conductivity type and a dopant concentration; and

a second region of the first conductivity type that contacts the buried layer and the first region, the second region having a dopant concentration that is less than the dopant concentration of the buried layer;

a third region of the second conductivity type formed in the second region, the third region contacting the top surface of the second region; and

a fourth region of the first conductivity type formed in the second region, the fourth region contacting the top surface of the second region and being spaced apart from the third region.

2. The rectifier of claim 1 and further comprising a fifth region of the second conductivity type formed in the second region, the fifth region contacting the top surface of the second region, the fourth region lying between the third and fifth regions.

3. The rectifier of claim 2 wherein the fifth region contacts the first region.

4. The rectifier of claim 2 wherein the fifth region is spaced apart from the buried layer.

5. The rectifier of claim 2 wherein the third region is spaced apart from the first region.

6. The rectifier of claim 2 wherein the first region lies vertically below the fifth region.

7. The rectifier of claim 2 wherein the fourth region is spaced apart from the buried layer.

8. The rectifier of claim 2 and further comprising:

a first conductive region that contacts the third region; and

a second conductive region that contacts the third region, the second conductive region being spaced apart from the first conductive region.

9. The rectifier of claim 8 wherein the first conductive region has the first conductivity type, and the second conductive region has the second conductivity type.

10. The rectifier of claim 9 wherein the first and second conductive regions are electrically connected together.

11. The rectifier of claim 8 and further comprising a third conductive region that contacts the fourth and fifth regions.

12. The rectifier of claim 11 wherein the third conductive region is spaced apart from the first and second conductive regions.

13. The rectifier of claim 11 and further comprising:

a layer of isolation material formed over the second region;

a first contact formed through the layer of isolation material to make an electrical connection with the first conductive region;

a second contact formed through the layer of isolation material to make an electrical connection with the second conductive region; and

a third contact formed through the layer of isolation material to make an electrical connection with the third conductive region.

14. A method of forming a silicon controlled rectifier comprising the steps of:

forming a semiconductor region, the semiconductor region having:

a buried layer having a first conductivity type and a dopant concentration;

a first region having a second conductivity type and a dopant concentration; and

a second region of the first conductivity type that contacts the buried layer and the first region;

forming a third region of the second conductivity type in the second region; and

forming a fourth region of the first conductivity type in the second region, the fourth region being spaced apart from the buried layer and the third region, and lying vertically over the buried layer.

15. The method of claim 14 wherein the step of forming a semiconductor region includes the steps of:

implanting a substrate of a second conductivity type with a dopant of the first conductivity type to form the buried layer;

implanting the substrate with a dopant of the second conductivity type to form the first region, the first region contacting the buried layer; and

growing an epitaxial layer of the first conductivity type on the substrate to form the second region.

16. The method of claim 14 wherein the first region is isolated from the substrate by the buried layer.

17. The method of claim 14 wherein the step of forming a semiconductor region includes the steps of:

growing an epitaxial layer of the second conductivity type on a substrate of the first conductivity type;

implanting the epitaxial layer with a dopant of the first conductivity type to form the buried layer;

implanting the epitaxial layer with a dopant of the second conductivity type to form the first region, the first region contacting the buried layer; and

implanting the epitaxial layer with a dopant of the first conductivity type to form the second region.

18. The method of claim 14 and further comprising the step of forming a fifth region of the second conductivity type in the second region, the fifth region contacting the fourth region.

19. The method of claim 18 wherein the fifth region contacts the first region.

20. The method of claim 18 wherein the fourth region lies between the third region and the fifth region.

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